NO.85-06 I

YM3805

Signal Processor & Controller for Compact Disc Player (SPC)

■ OUTLINE

The YM3805 is a compact disc player signal processor (SGP) and servo controller CMOS LSI developed by Yamaha.

The YM3805 carries out the digital filtering and other signal processing useful for optical pick-up EFM signal demodulation and erroneous signal detection and correction and improved audio quality, as well all servo control (e. g., focus, disc, tracking, feed).

It is used in conjunction with the special serial input DAC YM3015 or YM3020.

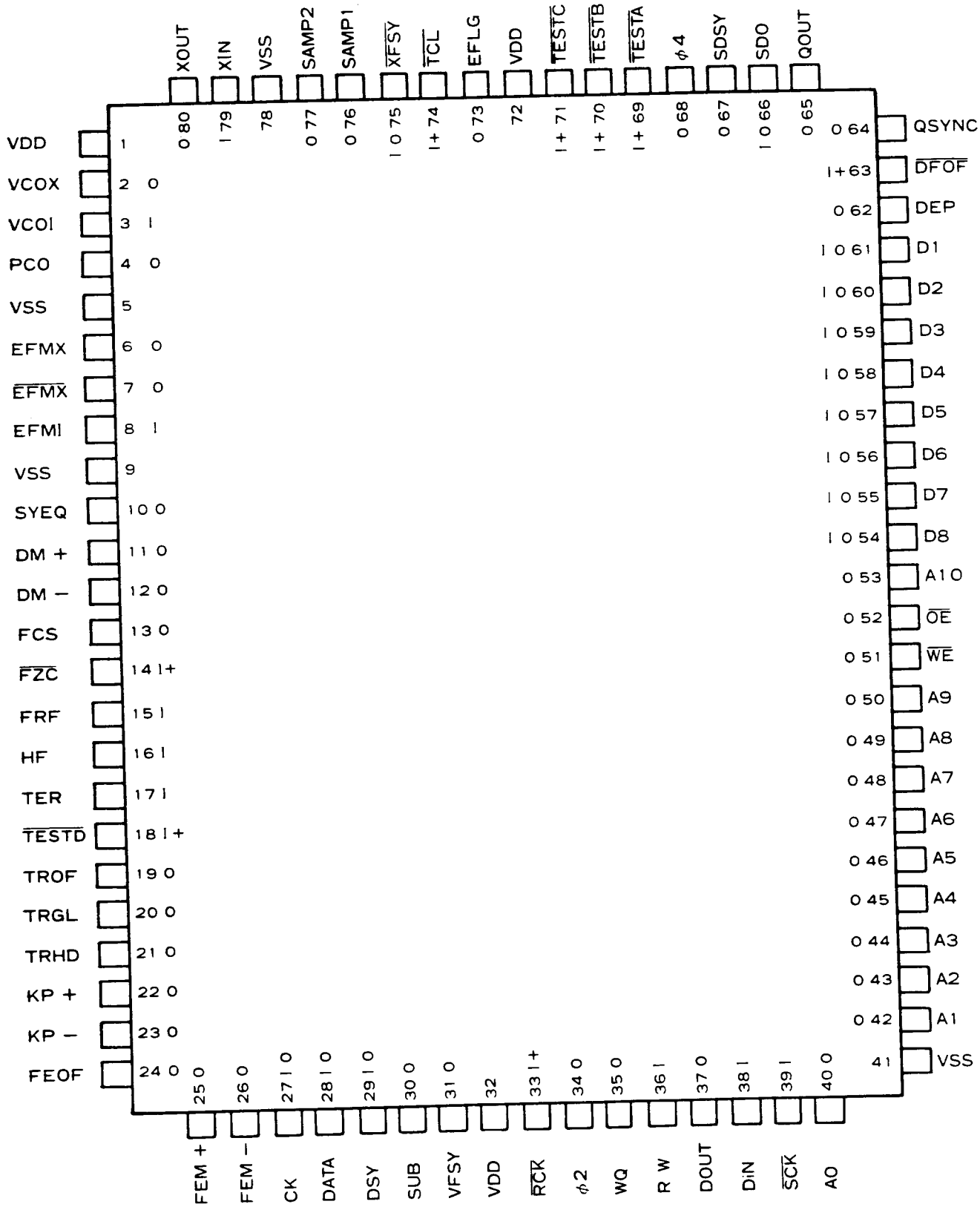
■ FUNCTIONS

1. Simple external connection of a crystal activates reference clock oscillations and the necessary internal timing signals.
2. Digitalizes the EFM signal, and based on that carries out clock playback and synchronizing signal isolation.
3. EFM demodulates this digital signal.
4. Isolates the Q sub-code from the EFM demodulated signal and, after carrying out a CRC check, outputs it to an external microprocessor.
5. Outputs a frame phase difference signal derived from the replayed clock and the reference clock and controls the rotation speed of the disc motor.
6. Carries out tracking as well as feed servo control for calling up the beginning of a selection and for fast forward, etc., upon input of a command from an external microprocessor.
7. Uses EFM demodulated signal buffering to absorb fluctuations in the rotation of the disc and interfaces the external RAM and signals (±4 frame jitter absorption).
8. Carries out unscrambling and de-interleaving of EFM demodulated signals in a set order.
9. Detects erroneous signals and corrects them and performs flag processing as well (double-error correction).
   Performs signal compensation, hold, and even muting.
10. Carries out digital filtering (signal break at 20 KHz) by doubling the sampling period (88.2 KHz for both the left and right channels), outputting a DAC signal. (Modes in which digital filtering is not carried out are also available.)

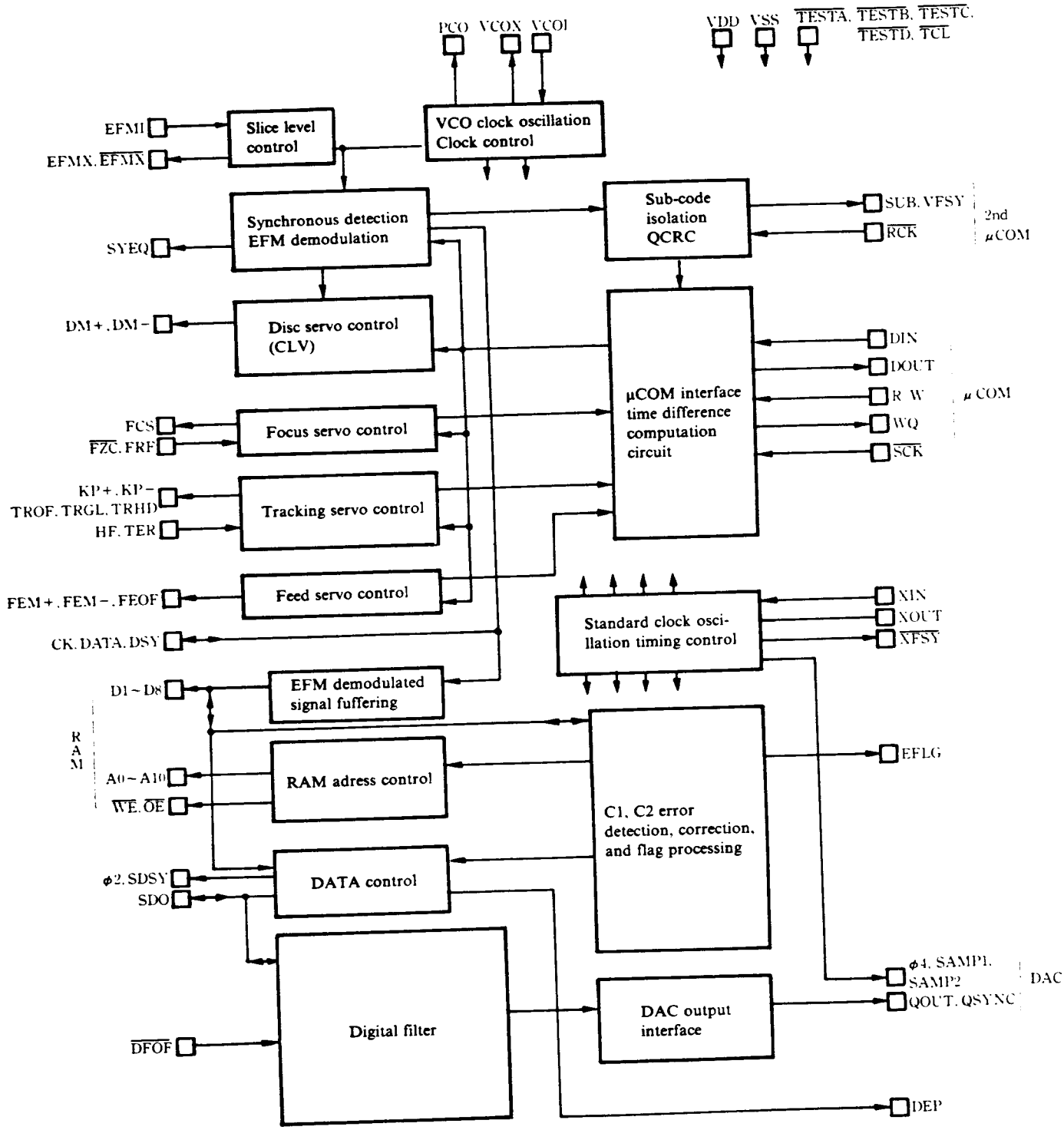
■ FEATURES

1. Silicon gate CMOS construction
2. 80 pin flat plastic package (saves space)
3. 5 V single power supply

■ TERMINAL DIAGRAMS



■ BLOCK DIAGRAM



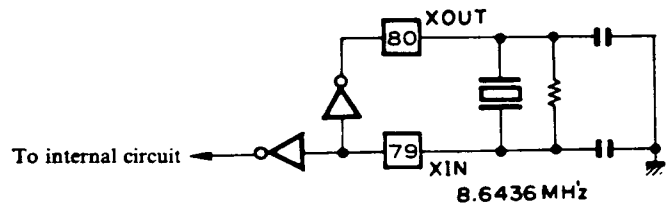
■ MAIN FUNCTIONS

- Clock oscillation (Crystal)
- Timing control
- Clock playback (VCO)
- Synchronous detection
- EFM signal demodulation
- Sub-code output
- Q code CRC
- μCOM interface
- Focus servo control
- Disc servo control
- Tracking servo control
- Feed servo control
- EFM demodulated signal buffering
- RAM adress control (±4 frame jitter absorption)
- C1, C2 error detection, correction, and flag processing
- DATA control (compensation and muting)
- Dital filtering
- DAC output

■ PIN FUNCTIONS

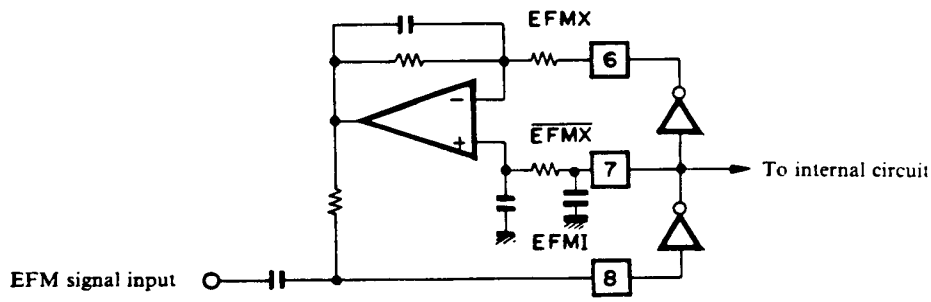
1. Clock Oscillation 79 XIN, 80 XOUT

Oscillation is obtained by connecting crystal oscillators (8.6436 MHz) between the two terminals and between the terminals and GND, with capacities of 20PF.



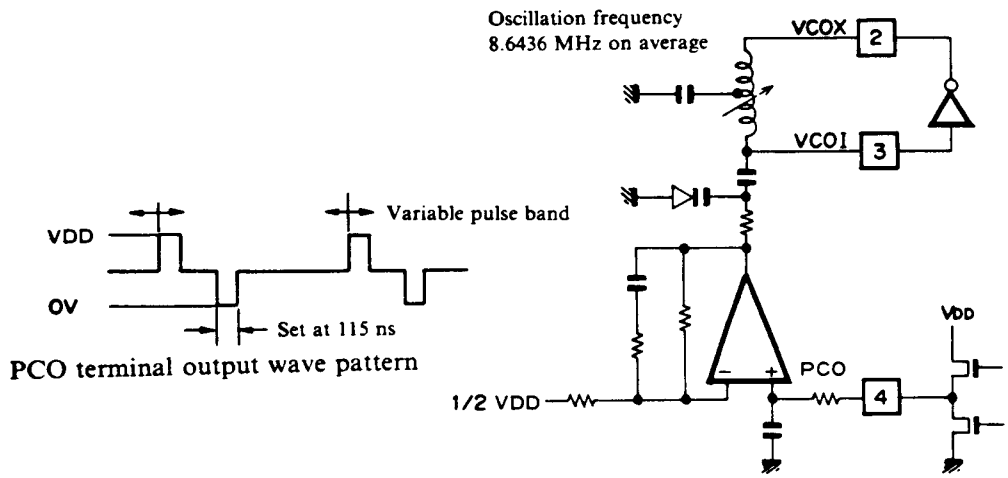
2. EFM Signal External Circuit 8 EFMI, 7 $\overline{\text{EFMX}}$, 6 EFMX

Inputs an appropriate level (1-2 VPP) optical pick-up signal at the EFMI terminal. Oscillation band limited reciprocally antiphase signals are generated from $\overline{\text{EFMX}}$ and EFMX. These carry out slice level control.



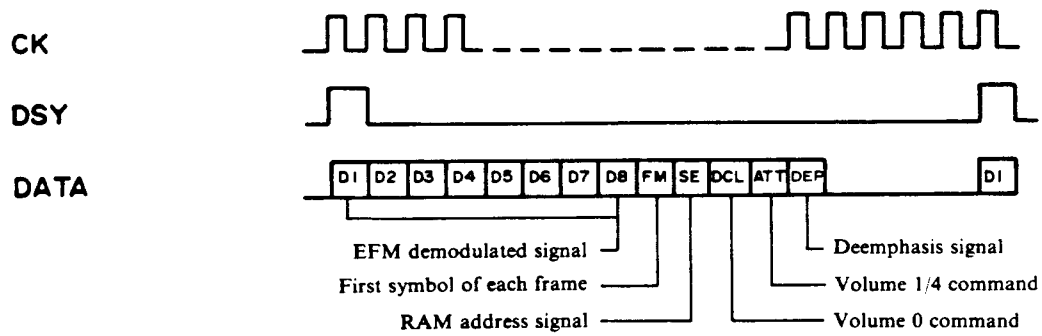
3. Clock Playback Circuit 4PCO, 3 VCOI, 2VCOX

Connecting an LC resonance circuit between VCOI and VCOX carries out clock oscillation (8.6436 MHz on average). The PCO terminal output is the phase difference of the clock and EFM pattern at polarity switchover. This unit is equipped with a variable capacity diode to boost the frequency when the polarity is positive, enabling playback of the clock.

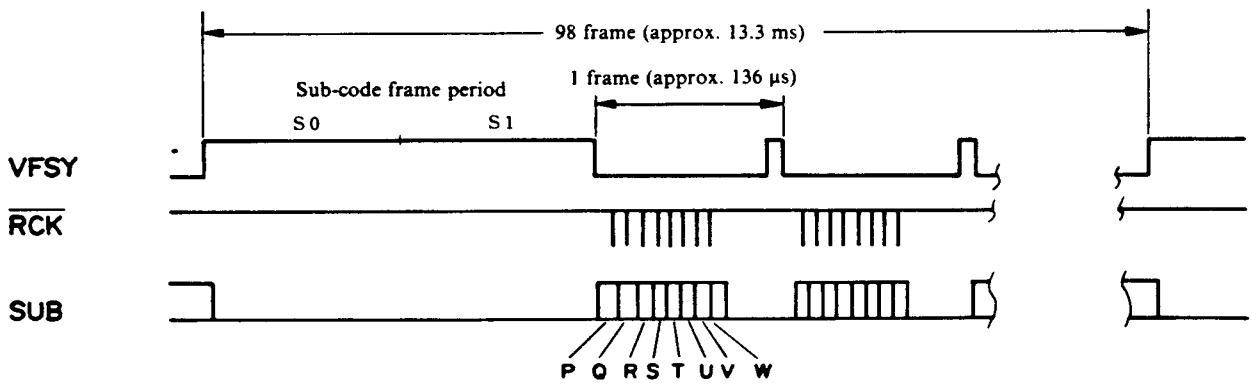


4. **Synchronized Uniform Signal 10 SYEQ**
   This terminal is used to check that "H" is obtained when the synchronizing signal detected from the EFM pattern and the internal counter synchronizing signal coincide.

5. **EFM Demodulated Signal Check Test Output 27 CK, 28 DATA, 29 DSY**
   CK denotes the clock that divides the VCO into 2; 4.3218 MHz on average. DATA consists of this clock's Bit Rate serial signal; the 17 Bit length includes EFM demodulated signal (8 Bits) and data control signal (5 Bits). DSY is the synchronizing signal that goes to "H" when timing coincides with peak signal. These 3 terminals are used for testing.



6. **Sub-code Output 30 SUB, 31 VFSY, 35 $\overline{\text{RCK}}$**
   VFSY is the synchronizing signal output that combines the frame and the sub-code frame (98 frame). A change from "H" to "L" in this signal is picked up externally and, when an 8-rotation clock is transmitted to the $\overline{\text{RCK}}$ terminal, the sub-code P~W can be read into the bit serial from the SUB output terminal.



7. Q Code Output System 35 WQ, 36 R/W, 37 DOUT, 39 $\overline{SCK}$

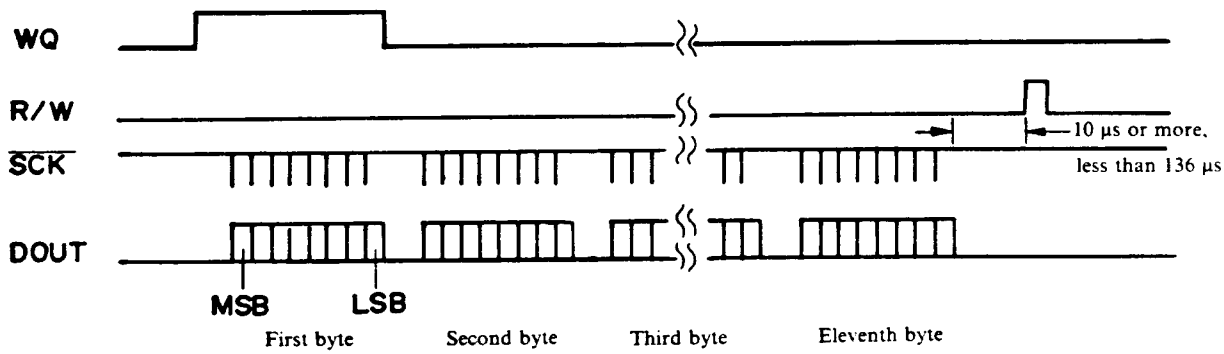
DOUT Contents

1	Internal STATE
2	CONT | ADR
3	TNO
4	X
5	MIN
6	SEC
7	FRAME
8	P−CODE
9	AMIN
10	ASEC
11	AFRAME

MSB							LSB
SIGN	S2	S1	8F	4F	MZ	FCO	NQ

SIGN : Search polarity
S2, S1 : Search mode
8F, 4F : Frame slippage
MZ : Disc motor stop
FCO : Focus out
NQ : New Q code

With μCOM, if WQ "H" is detected and an $\overline{SCK}$ transmitted, the above data can be read into the bit serial from the DOUT. Returning R/W to "H" after $\overline{SCK}$ clock transmission completes the process.



8. μCOM Command System 36R/W, 38DIN, 39$\overline{SCK}$

DIN contents

1	Command
2	μMIN
3	μSEC
4	μFRAME

Target time

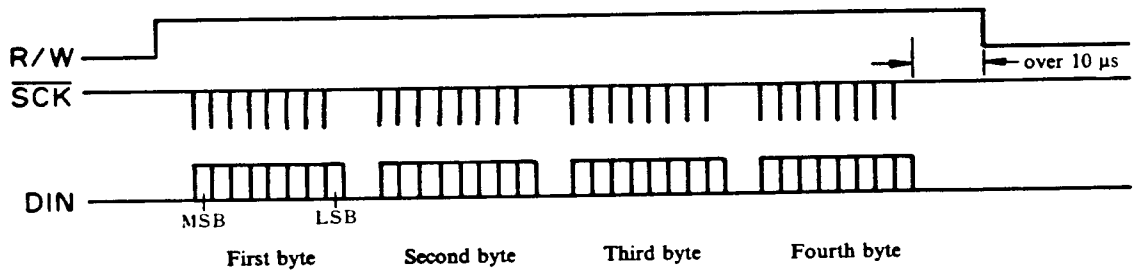
MSB

M4	M3	M2	M1	T4	T3	T2	T1
COMMAND				TEST			

0	0	0	X	0	STOP
0	0	1	0	1	FEED FORWARD
0	0	1	1	1½	FEED RETURN
0	1	0	X	2	FOCUS START
0	1	1	0	3	DISC START
0	1	1	1	3½	DISC BRAKE
1	0	0	0	4	PLAY
1	0	0	1	4½	PLAY MUTE
1	0	1	0	5	FF
1	0	1	1	5½	FB
1	1	0	0	6	FFF
1	1	0	1	6½	FFB
1	1	1	X	7	SEARCH (PAUSE)

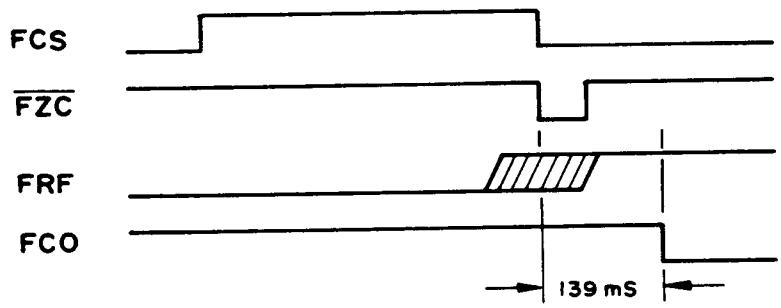
With μCOM, if $\overline{SCK}$ clock and DIN are synchronized and transmitted after R/W is set to "H", the above data can be input. When the command is any other than 7, 1 byte is input; when the command is 7, 4 bytes are input.

It is necessary to input an SPC initializing command ("H" for T4, otherwise "L") after the power has been turned on.



9. Focus Servo System Input 14$\overline{\text{FZC}}$·15FRF, Output 13FCS

These terminals are to be used for drawing in the focus servo.
The FCS signal is the signal that draws in the focus. When the point of focus is reached, the drawing in is halted if an $\overline{\text{FZC}}$ signal is activated and an FCO flag is dropped upon receipt of an FRF signal detecting a reflection.

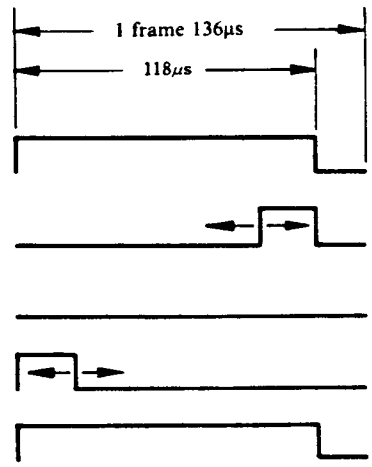


10. Disc Servo System 11DM+, 12DM−

DM+ and DM− take 1 frame as their period and constitute the PWM output. Entering DM+ and DM− at the same time does not obtain "H".
Under the stable PLAY conditions, a resolution of 925 ns, or 1/147 of a frame, obtains.

Command and disc servo internal mode and output combinations

COMMAND	0,1	2	3-0	3-½	4～7			DM ± SIGNAL
MODE	OFF	HOLD	ACC	BRK	ACC	AFC	PLL	DUTY
DM +			○		○	○	○	128/147
DM + (PWM)		○					○	1～127/147
NO OUTPUT	○		○	○	○	○	○	0
DM − (PWM)							○	1～127/147
DM −				○		○	○	128/147

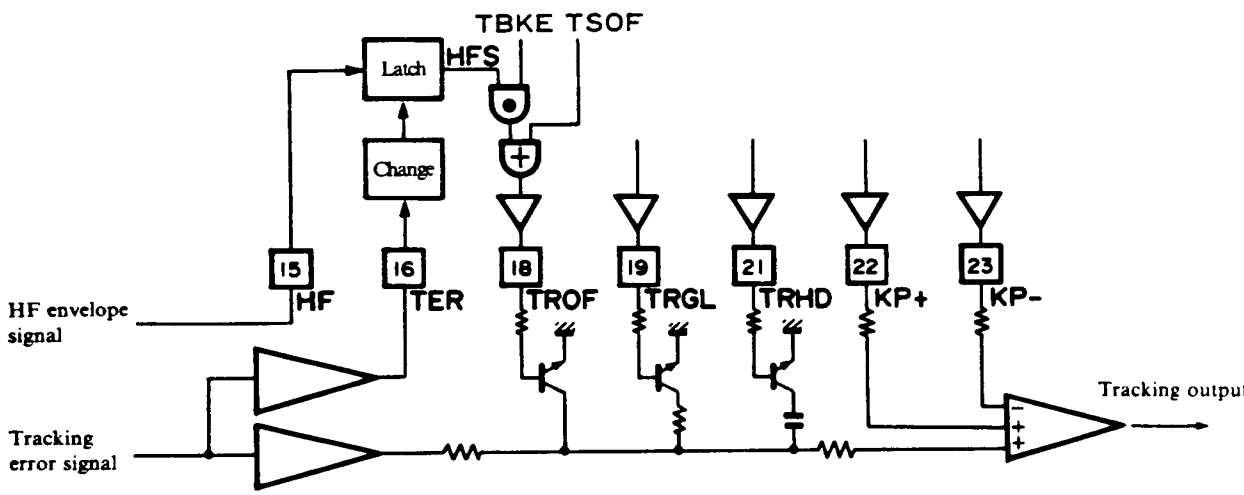


11. Tracking Servo System Input 16 HF, 17 TER
Output 19TROF, 20TRGL, 21 TRHD, 22 KP+, 23KP−

Samples changes in HF signal oscillation band at tracking error signal TER zero gross point when cross-cutting a track under search and outputs a TROF signal. The servo comes on and goes off depending on changes in the level of this signal, thereby easily controlling the track.

Outputs KP+ or KP− to carry out tracking, outputting TRHD during this time and holding the tracking error signal.

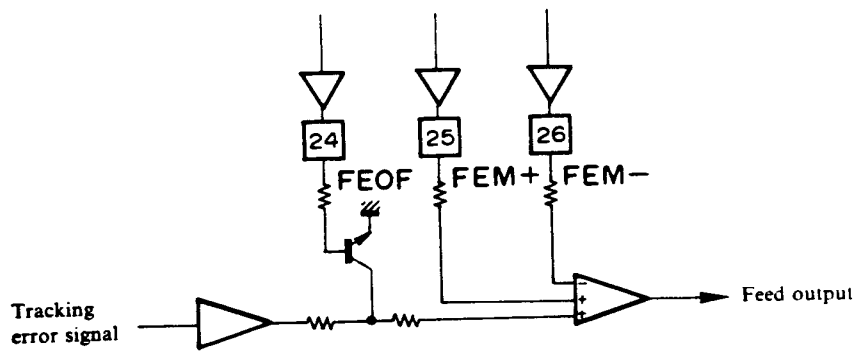
The TRGL signal is designed to increase tracking gain after kick completion.



Command	0,1,2,3,4	5-0	5-½	6-0	6-½		
Pattern (fast forward repetition)	(time units in milliseconds)	104	47.9	104	104		
TSOF TBKE TRGL TRHD KP+ KP−							
Pattern (repetition rotations vary with search mode time difference)	(time units in milliseconds)	.272 .544 7-1 17.4	.272 .544 7-4 7-5 17.4	.816 1.497 7-2 17.4	.816 1.497 7-6 17.4	2.993 5.714 7-3 34.8	2.993 5.714 7-7 34.8
Command search mode (time difference expressed in seconds)	7-0 (~+¼)	7-1 (+¼~4)	7-4 (~−¼) 7-5 (−¼~4)	7-2 (+4~128)	7-6 (−4~128)	7-3 (+128~)	7-7 (−128~)

12. Feed Servo System 24FEOF, 25 FEM+, 26FEM−

FEM+ and FEM− signals are output as high-speed feed signals. To cut off the feed servo during this time, an FEOF signal is output.

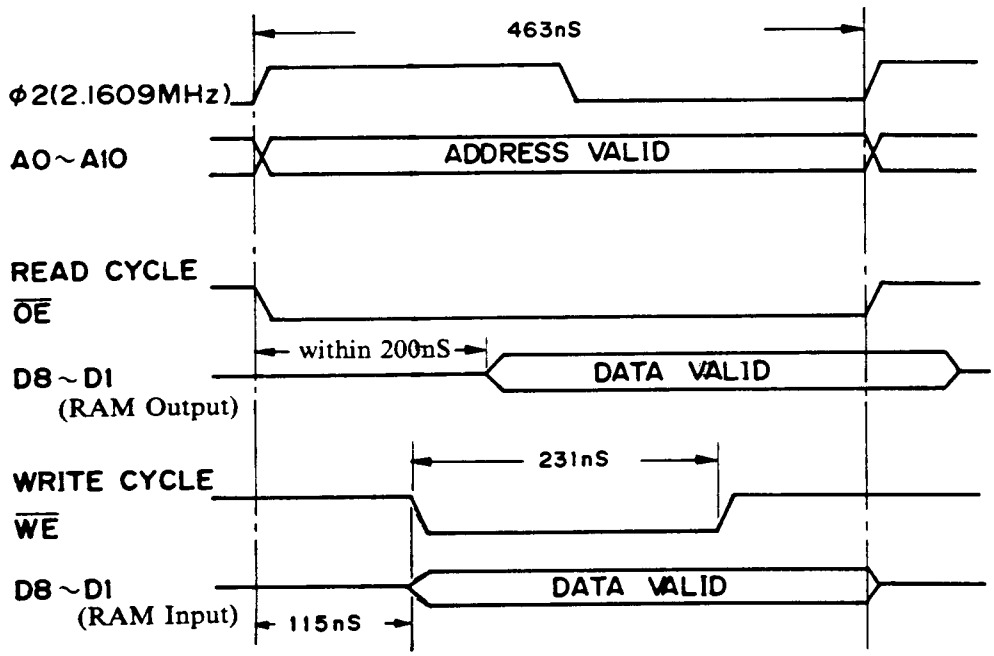


Command	0,2,3	1-0	1-½	4,5,6		
FEOF FEM+ FEM−						
Pattern (repetition rotations vary with serch mode time difference)				(time units in milliseconds)	34.8	34.8
Command search mode				7-0, 1, 2 7-4, 5, 6	7-3	7-7

13. RAM Connections 40A0~53A10, 51 $\overline{WE}$, 52 $\overline{OE}$, 54D8~861D1

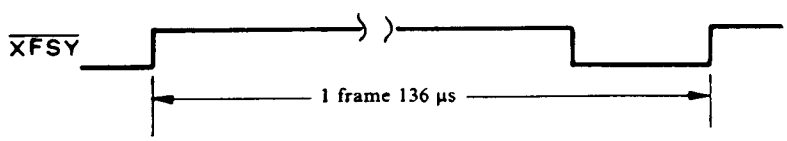
All are connected to the RAM and comprise the address, input control signals, and data signals.

SPC is outputting when $\overline{WE}$ = "L" and inputting when $\overline{WE}$ = "H".



14. Crystal Clock Synchronizing Signal 75 $\overline{XFSY}$

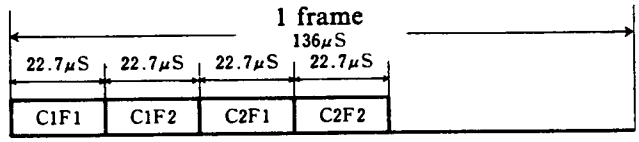
7.35 KHz frame synchronization signal.



15. C1, C2 Error Correction Check Test Signal 73 EFLG

This is the C1, C2 error correction circuit test terminal.

C1/C2	F2	F1
No error	0	0
Single-error correction	0	1
Double-error correction	1	0
Correction impossible	1	1



16. DATA Control Circuit and Serial Signal Output 34 φ2, 66 SDO, 67 SDSY, 69 TESTA 71 $\overline{\text{TESTC}}$

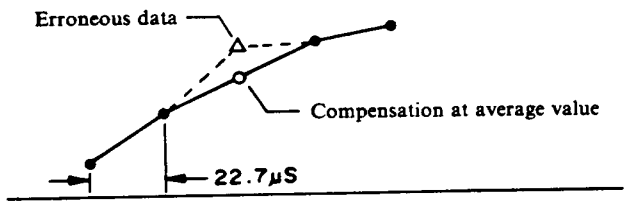
φ2 denotes 2.1609 MHz crystal clock.

SDO uses φ2 Bit Rate DAC serial output signals; left channel 24 Bit, right channel 25 Bit, LSB first.

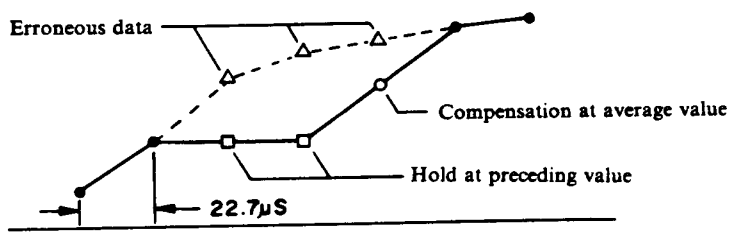
$\overline{\text{TESTA}}$ and $\overline{\text{TESTC}}$ are normally conducted on "H" and the SDO on output; on $\overline{\text{TESTA}}$ = $\overline{\text{TESTC}}$ = "L" with the same format, input is available to the digital filter.

SDSY is the synchronizing signal. SDO is "H" for the left channel and "L" for the right channel.

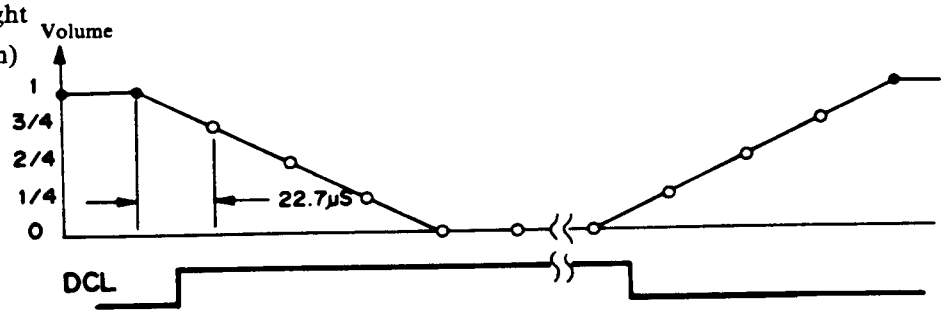
For discrete erroneous data (left and right channels independent)



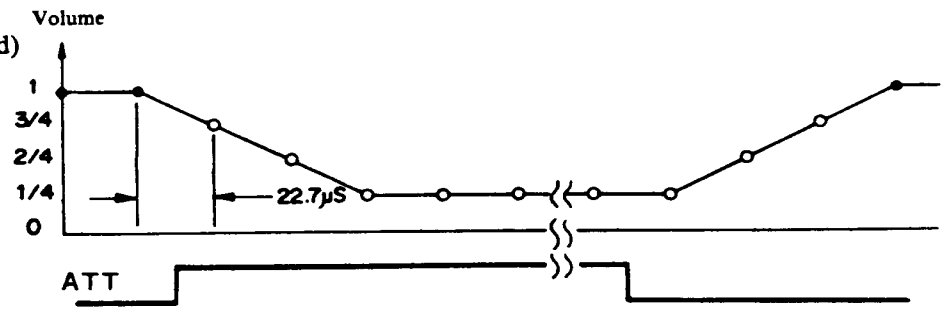
For continuous erroneous data (left and right channels independent)



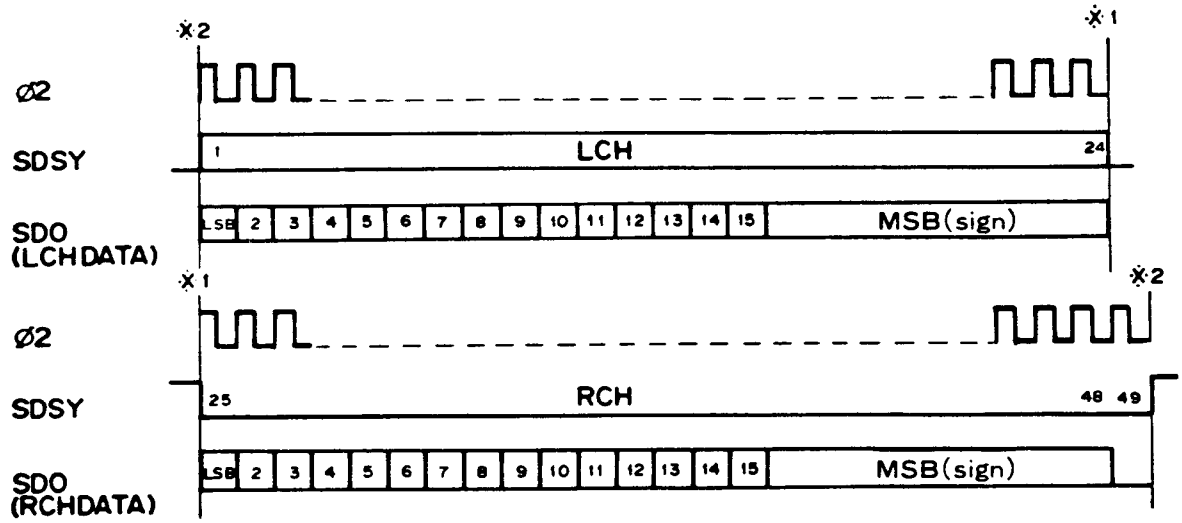
DCL (volume 0 command) (left and right channels in tandem)



Change in ATT
(Volume 1/4 Command)
(left and right
channels in tandem)

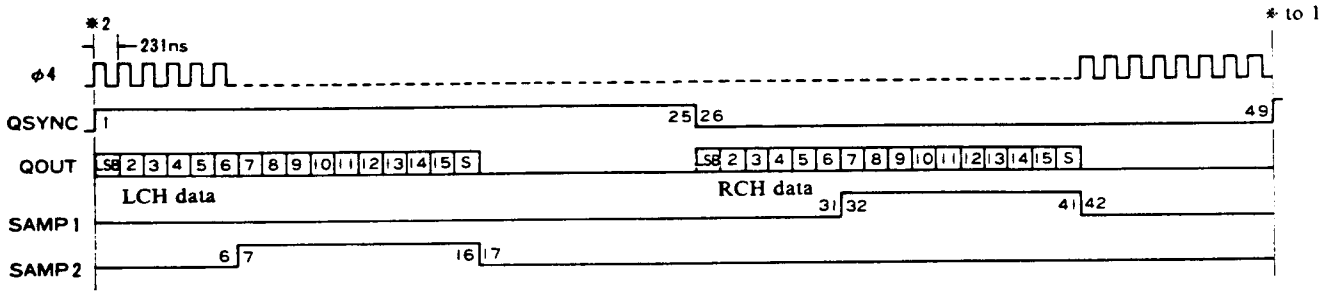


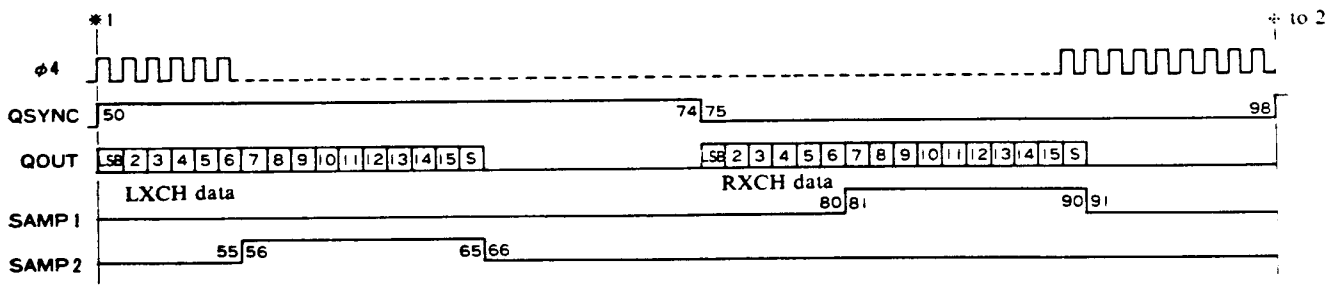
Serial Output Signal Format



17. DAC Interface 65QOUT, 64 QSYNC, 76 SAMP1, 77 SAMP2, 68 ϕ4, 63 $\overline{\text{DFOF}}$

The DAC serial output signal QOUT is 16 bit serial data synchronized to a 4.3218 MHz (ϕ 4) build-up and output by a 2's Comp format. (Refer to the diagram. The LX channel and RX channel show data that has been compensated by means of digital filtering.)
When the $\overline{\text{DFOF}}$ terminal is open, the data rate is 88.2 KHz (44.1 KHz plus or minus 20 KHz band suppression) for L ch and LX ch as well as for R ch and RX ch.
When $\overline{\text{DFOF}}$ terminal "L", LX = L, RX = R; offootivo data rate is 44.1 KHz.
QSYNC is the output synchronizing signal and denotes the L and LX output period when "L" and R and RX output period when "H" SAMP 1 and SAMP 2 are the L and R channel sampling signals.





18. **Deemphasis Signal 62DEP**
Deemphasis is necessary when the frequency characteristics control signal is "H".

19. **Test Terminals 69 $\overline{\text{TEST A}}$, 70 $\overline{\text{TEST B}}$, 71 $\overline{\text{TEST C}}$, $\overline{\text{TEST D}}$, 8 $\overline{\text{TCL}}$**
These comprise the several test terminals and normally read "H" with PULL-UP resistance. They need not be connected.

■ ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

ITEM	SYMBOL	RATING	UNITS
Supply voltage	V_{DD}	−0.3 ~ +7.0	V
Input voltage	V_I	−0.3 ~ V_{DD} +0.5	V
Operating temperature	Top	−20 ~ +75	°C
Storage temperature	Tstg	−50 ~ +125	°C

Recommended Operating Conditions

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNITS
Supply voltage	V_{DD}	4.75	5.00	5.25	V
Operating temperature	Top	0	25	75	°C

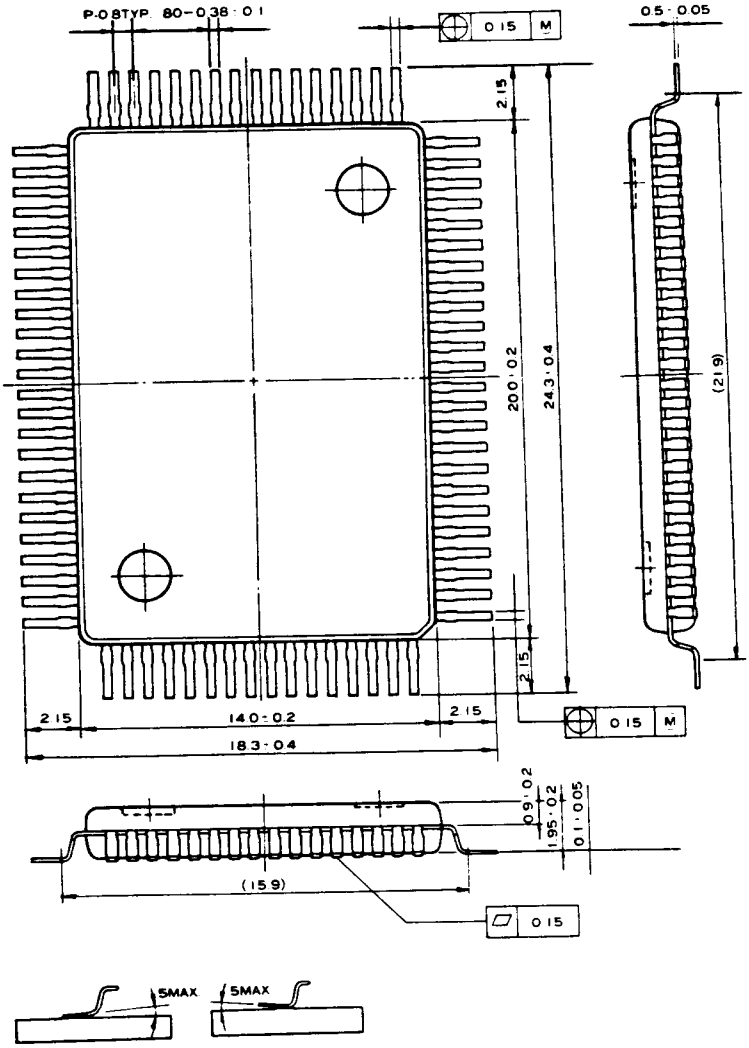
Electrical Characteristics

ITEM	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	REMARKS
Supply current	I_{DD}	V_{DD} = 5V		25	40	mA	
Output high level voltage	V_{OH}	I_{OH} = 20μA	4.0			V	
Output low level voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	
Input high level voltage (1)	V_{IH1}		3.5			V	(Note 1)
Input low level voltage (1)	V_{IL1}				1.5	V	(Note 1)
Input high level voltage (2)	V_{IH2}		2.0			V	(Note 2)
Input low level voltage (2)	V_{IL2}				0.8	V	(Note 2)
Input leakage current	I_{LK}	V_I = 5V			10	μA	

Condition: V_{DD} = 5.0V±5%, Top = +0 ~70°C

Note 1: Applicable to terminals 3.VCOI 8.EFMI 14.$\overline{\text{FZC}}$ 15.FRF 16.HF 17.TER.
Note 2: Applicable to terminals 33.$\overline{\text{RCK}}$ 38.DIN 39.$\overline{\text{SCK}}$ 54.D8- 61.D1.

■ OUTLINE DIMENSION



The specifications of this product are subject to improvement changes without prior notice.

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007694

0.4K-1007 Printed in Japan 85.11